Name Surname :

ID :

EE 213 Midterm Examination

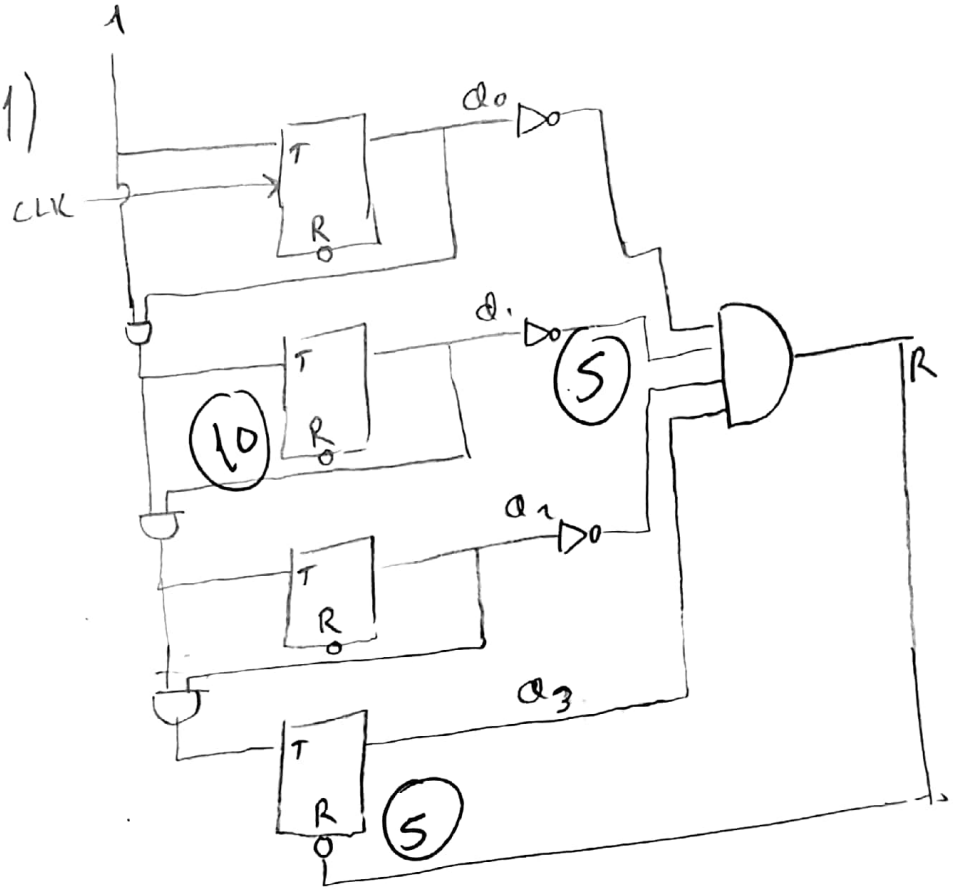
1) **20P** Design a counter that counts between 0 and 8 continiously such that, 0,1,2,3,4,5,6,7,8,0,1,2,3,4,5,67,8,0,1,2,3...
2) **15P** Please make the operations given below and calculate the results in binary form
   a) **8P** 67-78
   b) **8P** 78-67
   c) **4P** 67+78
3) **20P** Design a Full adder (Full adder adds 3 one bits) by using only NAND gates and INVERTERS.
4) **25P** Design a Full adder (Full adder adds 3 one bits) by using only DECODERS.
5) **20P** Design the circuit that implements the truth table given below

X	Y	Q(t)	Q(t+1)
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

23.11.17

EE 213 Midterm
2017-2018
SOLUTIONS

1)



2)

1 0 0 0 0 1 1	(67)
1 0 0 1 1 1 0	(78)
0 1 1 1 1 0 1	(-67)
0 1 1 0 0 1 0	(-78)

a) 1 0 0 0 0 1 1 (67)
+ 0 1 1 0 0 1 0 (-78) (5)

1 1 1 0 1 0 1

↳ no carry, by 2nd complement = 0 0 0 1 0 1 1
(-) = −11

b) $1\ 0\ 0\ 1\ 1\ 1\ 0$ (78)

$0\ 1\ 1\ 1\ 1\ 0\ 1$ (-67) (5)

$+$

$1\ 0\ 0\ 0\ 0\ 1\ 1$ → no need to 2nd comp

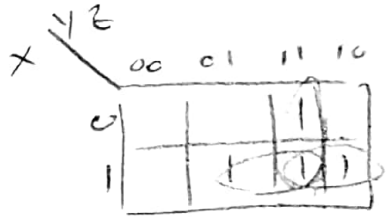
↳ carry indicates (+)

$= 11//$

3)

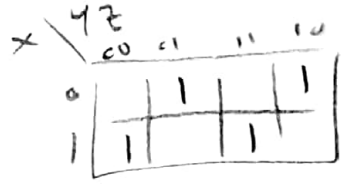
x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$S =$



$S = xz + xy + zy$ (10)

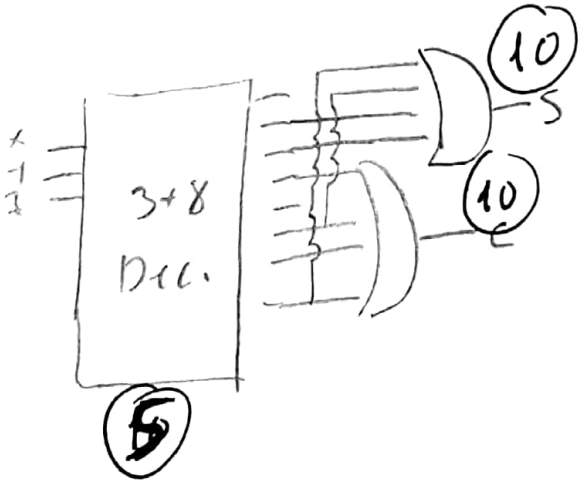
$C =$



(10)

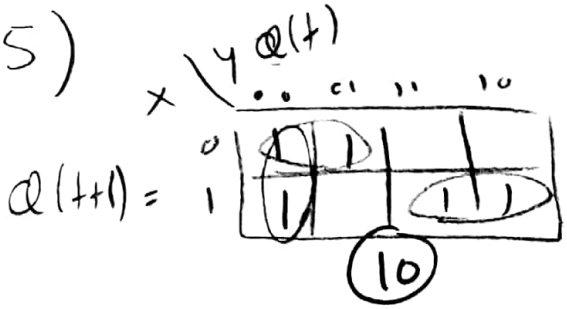
$C = x\bar{y}\bar{z} + \bar{x}y\bar{z} + xyz + \bar{x}y\bar{z}$

4)

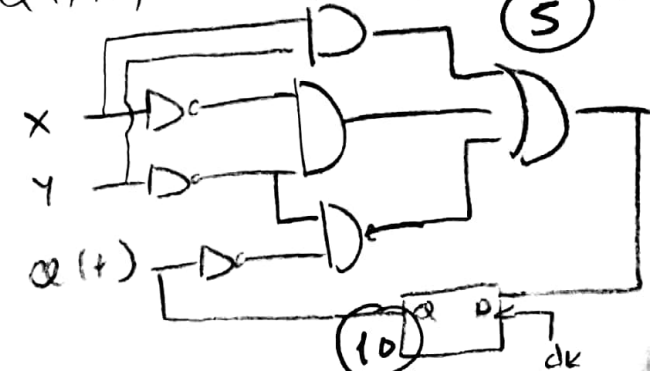


5)

$Q(t+1) =$



$Q(t+1) = \bar{x}\bar{y} + \bar{y}Q(t) + yx$



Name Surname : 15.11.2018

ID

FALL 2018 – 2019 EE 213 MIDTERM QUESTIONS

Q1) Please implement 34-78 operation in binary form and only as it appears.

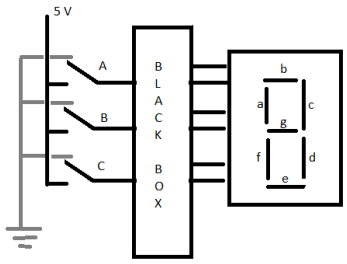
a) 5p Using the 1’st complement form
b) 5p Using the 2’nd complement form

Q2) F=x’ +xz’+yx

for the given expression F, please write the expression for b) and draw the circuit for a)

a) Using a decoder and any gate you want.
b) Using only NOR gates (no inverter usage is permitted)

Q3) Please design the smallest and fastest possible circuit in black box on the figure given below, such that only displaying Floors 0,1 and 3 are needed. It will display nothing at floor 2.



Q4) Design a circuit such that you have a button to select one of the operations of multiplication or addition, then it takes two 1 bit operands to operate the selected operation on them. Let the circuit finally show the 1’st complement of the result.

2018-2019 Fall

EE 213

Solutions

1) $34 = \underline{1}\,\underline{0}\,\underline{0}\,\underline{0}\,\underline{1}\,\underline{0}$ (32, 2)

$78 = \underline{1}\,\underline{0}\,\underline{0}\,\underline{1}\,\underline{1}\,\underline{1}\,\underline{0}$ (64, 8, 4, 2)

$-78 = 0\,1\,1\,0\,0\,0\,1$ 1's

$+\ 1$

$0\,1\,1\,0\,0\,1\,0$ 2's

a) $100010 + 010001$

$1\,0\,1\,0\,0\,1\,1$

$+\ 1$ (−)

$0\,1\,0\,1\,0\,0$

2nd comp

$1\,0\,1\,0\,1\,1$

$+\ 1$

$1\,0\,1\,1\,0\,0$

$32 + 8 + 4$ $= -44$

b) $100010 + 110010$

$1\,0\,1\,0\,0\,1\,0\,0$

2nd comp

$1\,0\,1\,0\,1\,1$

$+\ 1$

$1\,0\,1\,1\,0\,0$

(−) $32\ 8\ 4$

44

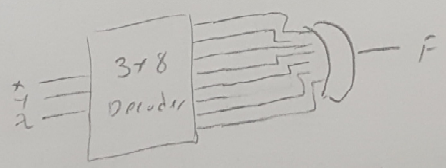
$= -44$

2) $F = x' + xz' + yx$

a) $F = x'(\bar{y}\bar{z} + \bar{y}z + y\bar{z} + yz) + x(y+\bar{y})z' + xy(z+\bar{z})$

$= \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}y\bar{z} + \bar{x}yz + xyz + x\bar{y}\bar{z} + xy\bar{z} + xyz$

$m_0 \quad m_1 \quad m_2 \quad m_3 \quad m_7 \quad m_4 \quad m_7 \quad m_6$



b) $F = (x' + xz' + yx)'' = (x \cdot (xz)' \cdot (xy)')'$ (11 ← added)

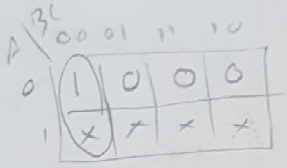
$= (x' \cdot (\bar{x}+z)' \cdot (\bar{x}+\bar{y}))'$

$= (x' + (\bar{x}+z)'' + (\bar{x}+\bar{y})'')'$

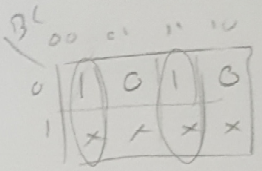
3)

A	B	C	a	b	c	d	e	f	g
0	0	0	1	1	1	1	1	1	0
0	0	1	0	0	1	1	0	0	0
0	1	0	0	0	0	0	0	0	0
0	1	1	0	1	1	1	1	0	1
1	0	0	x	x	x	x	x	x	x
1	0	1	x	x	x	x	x	x	x
1	1	0	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x

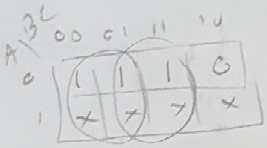
a =>



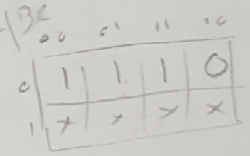
b =>



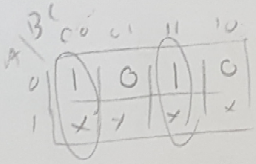
c =>



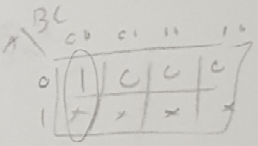
d =>



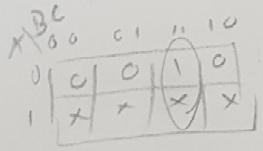
e =>



f =>



g =>



$a = \bar{B}\bar{C}$

$b = \bar{B}\bar{C} + BC$

$c = \bar{B} + C$

$d = \bar{B} + C$

$e = \bar{B}\bar{C} + BC$

$f = \bar{B}\bar{C}$

$g = BC$

$a = f$

$b = e$

$c = d$

4)

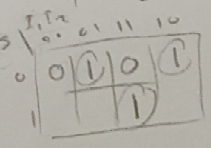
S	In_1	In_2	Q_2	Q_1
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	1

add

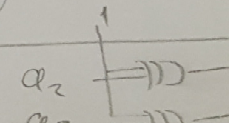
multip

$Q_2 = \bar{S}\, In_1\, In_2$

$Q_1 =>$



$= \Sigma(m_1, m_2, \ldots$



17.11.2020

EE 213 DIGITAL DESIGN

2020-2021

MIDTERM EXAMINATION

1) **25p** Please convert the expression F= x'y + yz' + z +x'yz to minterm represantation.
2) **25p** Please implement the simplest SOP implementation of the same expression F= x'y + yz' + z +x'yz using only NAND Gates.
3) **30p** Design a circuit that implements the same function = x'y + yz' + z +x'yz using a single multiplexer.
4) Calculate the given operations in binary form. (All calculations will be done in binary form)
   a) **7p** 23-37
   b) **7p** 30-28
   c) **6p** 35+43

17.11.2020

EE 213

2020 - 2021

FALL MIDTERM

SOLUTIONS

1) $F = x'y(z+z') + (x+x')yz' + (x'y' + x'y + xy' + xy)z + x'yz$

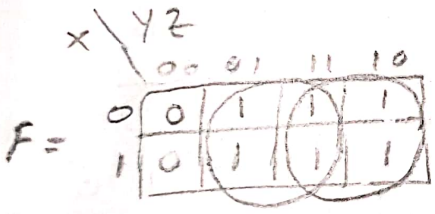
$F = x'yz + x'yz' + xyz' + x'yz' + x'y'z + x'yz + xy'z$

$+ xyz + x'yz$

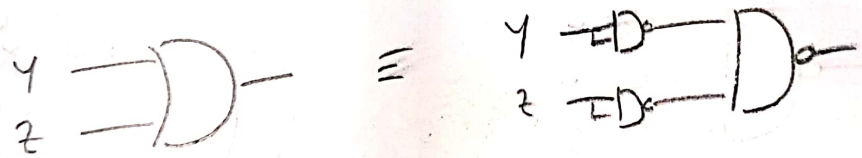
$F = \Sigma(3, 2, 6, 2, 1, 3, 5, 7, 3) = \Sigma($

$= \Sigma(1, 2, 3, 5, 6, 7)$

2)



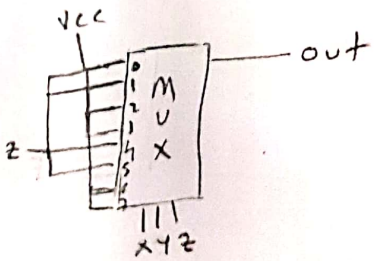
$F = Y + Z$



$F = (Y \cdot Y)' \cdot (Z \cdot Z)')'$

3)

X	Y	Z	F	
0	0	0	0	Z
0	0	1	1	
0	1	0	1	1
0	1	1	1	
1	0	0	0	Z
1	0	1	1	
1	1	0	1	1
1	1	1	1	



4) $\begin{array}{r} 0\ 1\ 0\ 1\ 1\ 1 \quad (23) \\ 1\ 0\ 0\ 1\ 0\ 1 \quad (\ ) \end{array}$

4) a) 0 1 0 1 1 1 (23)
1 0 0 1 0 1 (37) => 2's comp

1 1 1 1
0 1 0 1 1 1 (23)
+ 0 1 1 0 1 1 (-37)
---
1 1 0 0 1 0
=
↳ -(0 1 1 1 0) ← 2's comp

∴ = -14

b) 1 1 1 1 0 (30)
1 1 1 0 0 (28) =>

1 1 1 1 0
→ 0 0 1 0 0
2's comp +
---
* 0 0 0 1 0

↳ overflow ignored and positive

= +2

c) 1 0 0 0 1 1 (35)
1 0 1 0 1 1 (43)
+
---
1 0 0 1 1 1 0

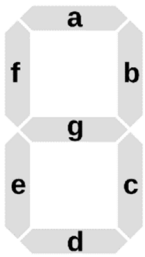
$(2^6+2^5+2^4+2^3+2^2+2^1+2^0) = +78$

Name Surname : **ID :** **25.11.2021**
Duration : 60 mins.

EE 213 Digital Design
2021 – 2022
MIDTERM EXAM

Q1) 30 p. Write the decimal number 498 in ;

a) Binary form
b) Octal form
c) Binary coded decimal form
d) Calculate 498-500 in binary form



Q2) 30 p Draw a 5 bits adder/subtructor circuit.

Q3) 40 p Assume we have a building that has 8 floors ; and a seven segment (given above) will be used to display the floor number on the display. Please find the MOST SIMPLIFIED ONY NAND circuit expression for LED “b” . Show all steps

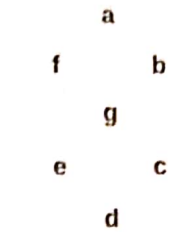
SOLUTIONS

Name Surname : SOLUTIONS ID : 27.11.2021 25.11.2021
Duration : 60 mins.

EE 213 Digital Design
2021 – 2022
MIDTERM EXAM

Q1) 30 p. Write the decimal number 498 in ;

a) Binary form
b) Octal form
c) Binary coded decimal form
d) Calculate 498-500 in binary form



Q2) 30 p Draw a 5 bits adder/subtructor circuit.

Q3) 40 p Assume we have a building that has 8 floors ; and a seven segment (given above) will be used to display the floor number on the display. Please find the MOST SIMPLIFIED ONY NAND circuit expression for LED "b" . Show all steps

SOLUTIONS

1)a) $(498)_{10}$ => 1 1 1 1 1 0 0 1 0

$498 = 256 + 128 + 64 + 32 + 16 + 2$

$2^8 + 2^7 + 2^6 + 2^5 + 2^4 + 2^1$

b) $(498)_{10} = (762)_8$

c) 4 9 8 = | 0100 | 1001 | 1000 |
4 9 8

d) 498 - 500 = 498 + (-500)

111110010 ← 498
111110100 ← 500

2's comp. ↓

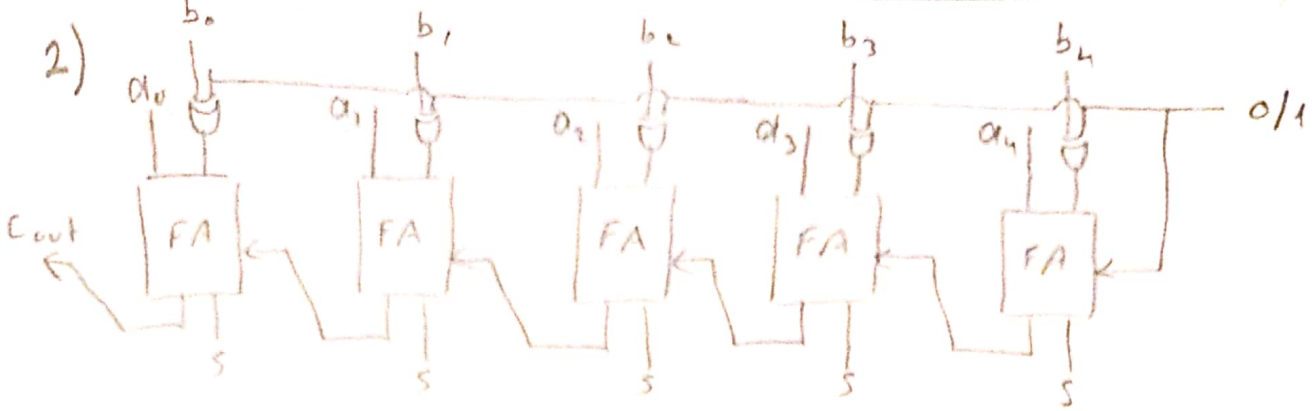
000001100 ← -500

111110010 498
+ 000001100 + -500

(1)111111110 → 2's comp

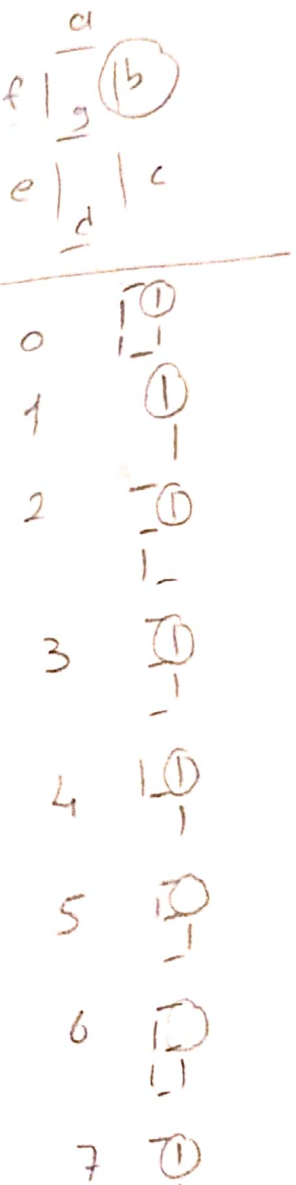
↳ (-) 000000010

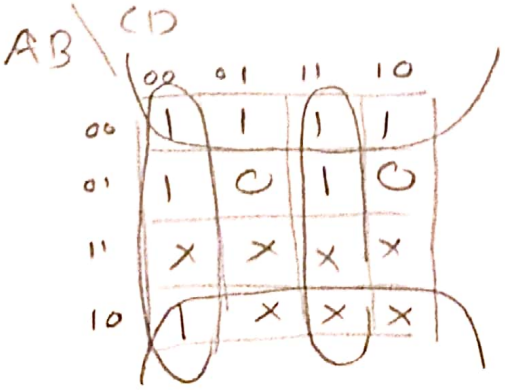
2)



3)

A	B	C	D	a	b	c	d	e	f	g
0	0	0	0		1					
0	0	0	1		1					
0	0	1	0		1					
0	0	1	1		1					
0	1	0	0		1					
0	1	0	1		0					
0	1	1	0		0					
0	1	1	1		1					
1	0	0	0		1					
1	0	0	1		x					
1	0	1	0		x					
1	0	1	1		x					
1	1	0	0		x					
1	1	0	1		x					
1	1	1	0		x					
1	1	1	1		x					





we wont have this for $\uparrow 4 = 1_{-1}$

$b = \bar{C}\bar{D} + CD + \bar{B}$

$b = ((\bar{C}\bar{D})' \cdot (C \cdot D)' + (B \cdot B)')'$

where  ≡

Name Surname : SOLUTIONS
ID

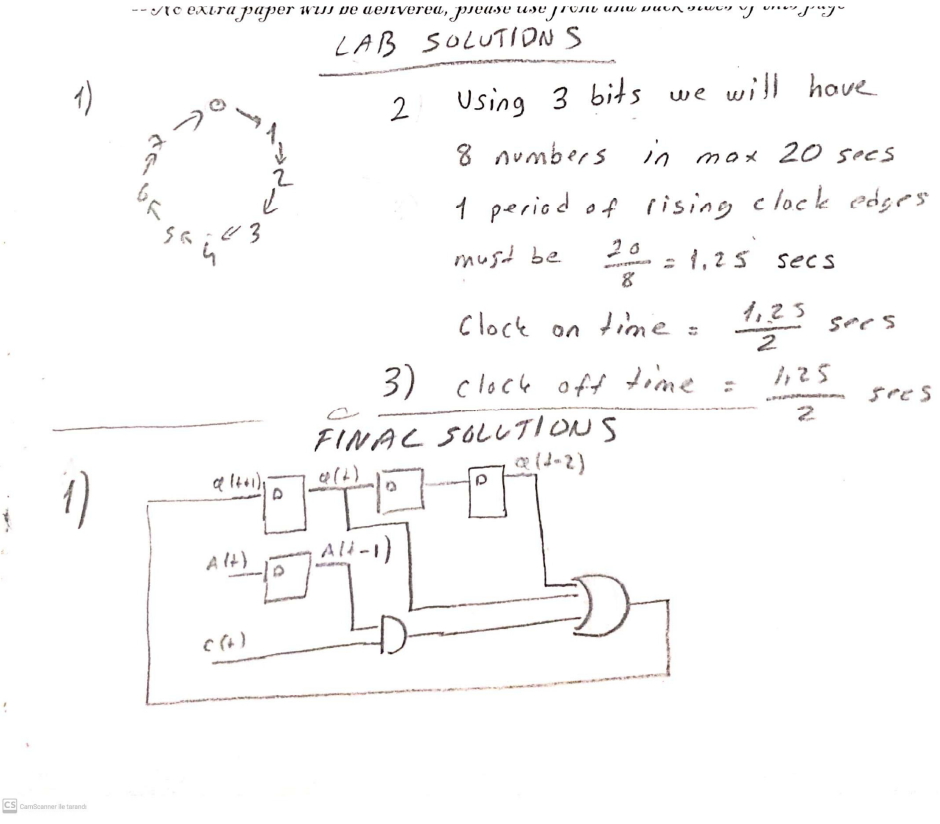
EE 213 LAB Exam 10.01.2022

1) Please draw the state diagram of a 3 bits counter such that it will give the outputs of one period in 20 seconds, and shows exactly one period on the screen.
2) To see the outputs exactly as above what value should the clock on time be adjusted to ?
3) To see the outputs exactly as above what value should the clock off time be adjusted to ?

EE 213 FINAL EXAM

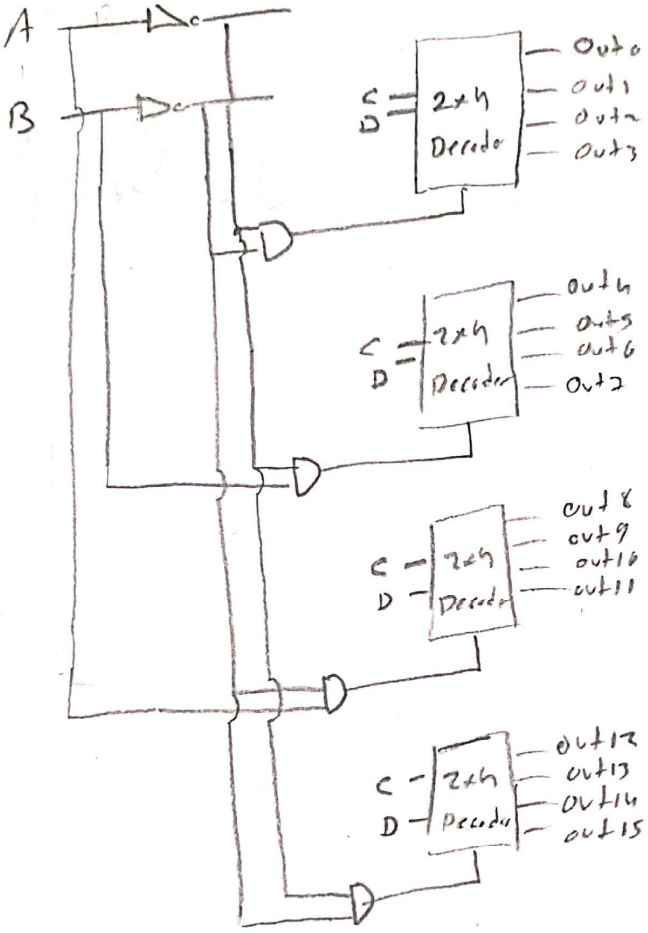
1) Draw the circuit for Q(t+1)=Q(t)+A(t-1).C(t)+Q(t-2)
2) Draw the state diagram of a 3 bits up/down counter.
3) Design a 4x16 decoder using four 2x4 Decoder

--No extra paper will be delivered, please use front and back sides of this page--



2)

3)


A
B
C
D
2x4
Decoder
out0
out1
out2
out3
out4
out5
out6
out7
out8
out9
out10
out11
out12
out13
out14
out15