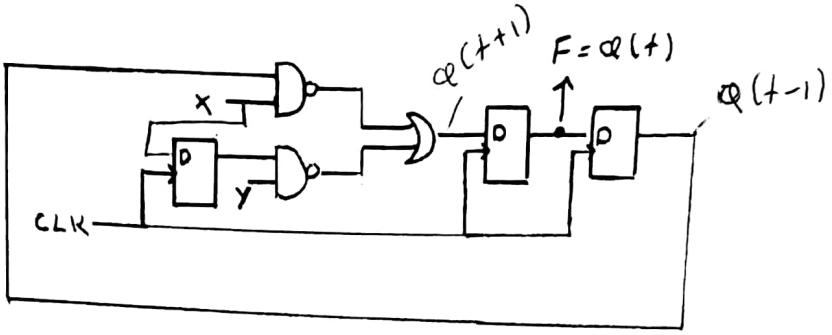
Name Surname: **ID :** **12.01.2018**

EE 213 FINAL EXAM

2017- 2018

Q1) (30p) Write the expression of thepoint F for the given circuit below.

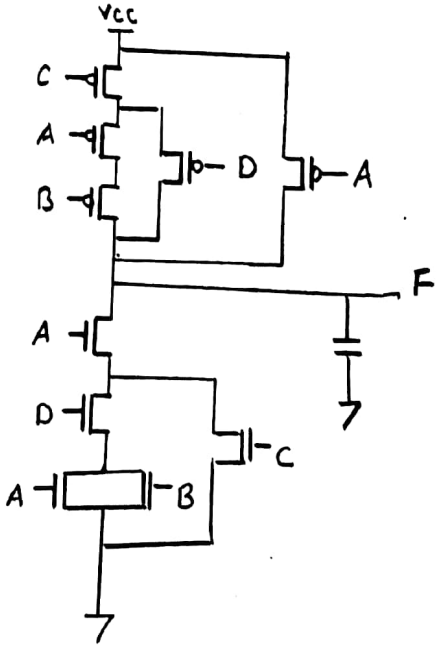


Q2) (25p) Design a 8x8 RAM and declare the necessary input,selections,control bits etc... on your design such that it will write the value of 243 to the address of "123".

Q3) Design the Circuit for F= ∑(1,3,7,8,10)

a) **(15p)** By using oly one multiplexer
b) **(10p)** By using only one decoder

Q4) (20p) Write the unsimplified expression for the gicen Complementary Metal Oxide Semiconducter (CMOS) circuit below.



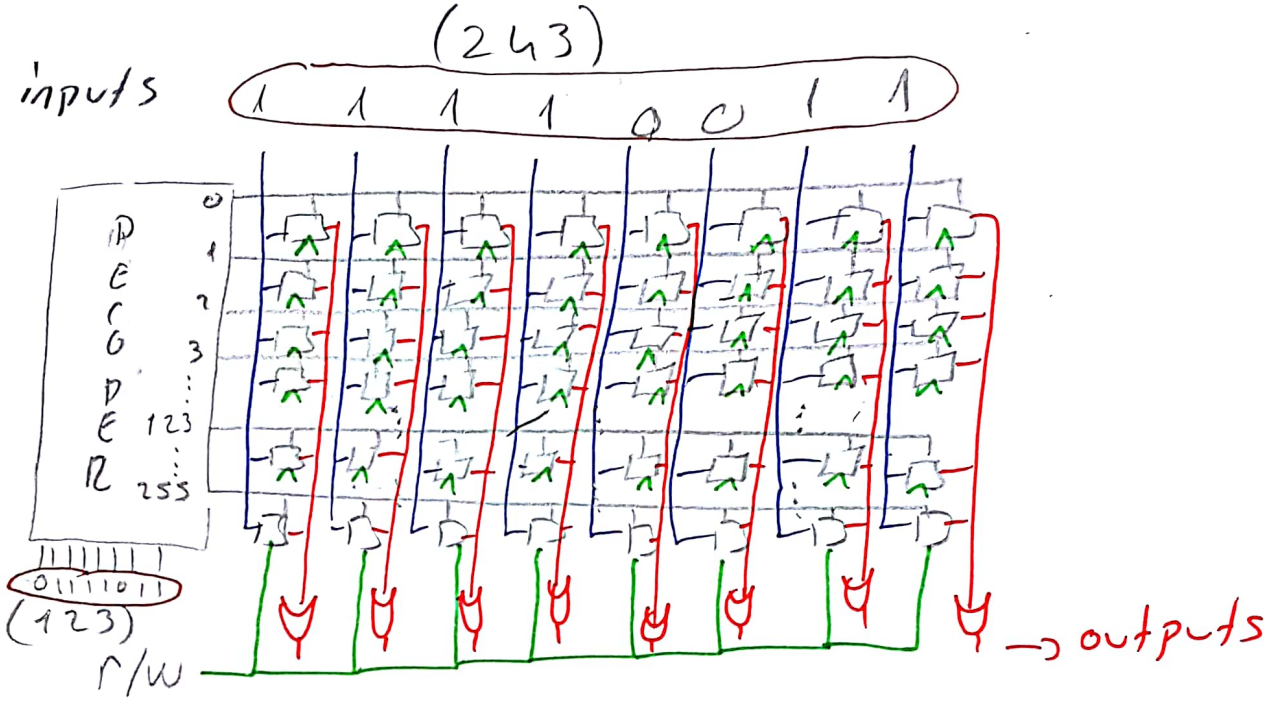
☺Good Luck ☺

EE 213 FINAL

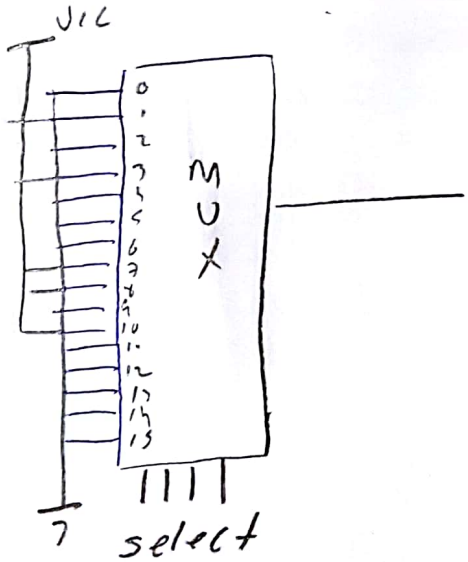
SOLUTIONS

1) $F = Q(t) = \overline{(Q(t-1) \cdot x(t-1))} + \overline{x(t-2) \cdot y(t-1)}$

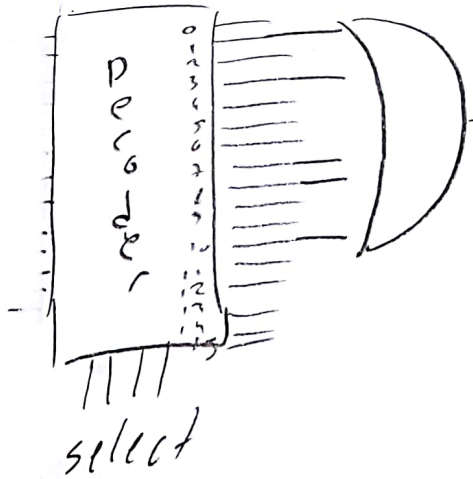
2)



3) a)



b)



4) $\overline{[[(A+B) \cdot D] + C] \cdot A} = F$

Name Surname : **ID :**

EE 213 Digital Design

FINAL EXAM

1) ***Design the circuit for Q(t+1)= Q(t-1) + Q(t)***
2) ***Design a counter that counts as 0,1,4,2,5,6, 0,1,4,2,5,6, …***
3) ***Design a circuit that implements F = xy +yz+ xz by using a multiplexer***
4) ***Design a 5x 32 multiplexer by using four 3x 8 multiplexer.***

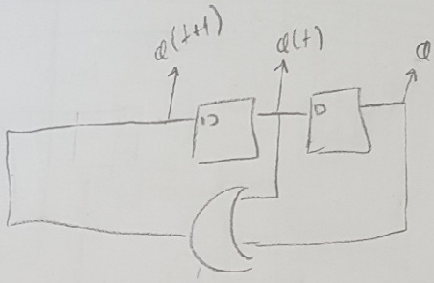
Name Surname : SOLUTIONS ID :

EE 213 Digital Design

FINAL EXAM

1) *Design the circuit for Q(t+1)= Q(t-1) + Q(t)*
2) *Design a counter that counts as 0,1,4,2,5,6, 0,1,4,2,5,6, ...*
3) *Design a circuit that implements F = xy +yz+ xz by using a multiplexer*
4) *Design a 5x 32 multiplexer by using four 3x 8 multiplexer.*

1)

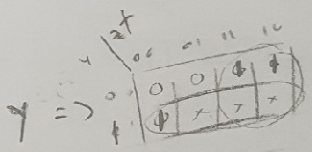


25

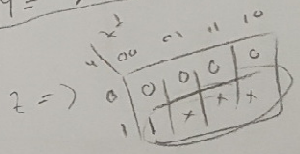
2)

y z t	y z T
0 0 0	0 0 0
0 0 1	0 0 1
0 1 0	1 0 0
0 1 1	1 0 1
1 0 0	1 1 0
1 0 1	x x x (Reset)
1 1 0	x x x
1 1 1	x x x
0 0 0	x x x
0 0 1	x x x
0 1 0	x x x
0 1 1	x x x
1 0 0	x x x
1 0 1	x x x
1 1 0	x x x
1 1 1	x x x

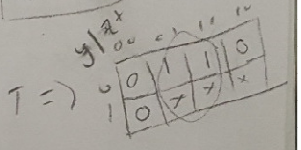
10



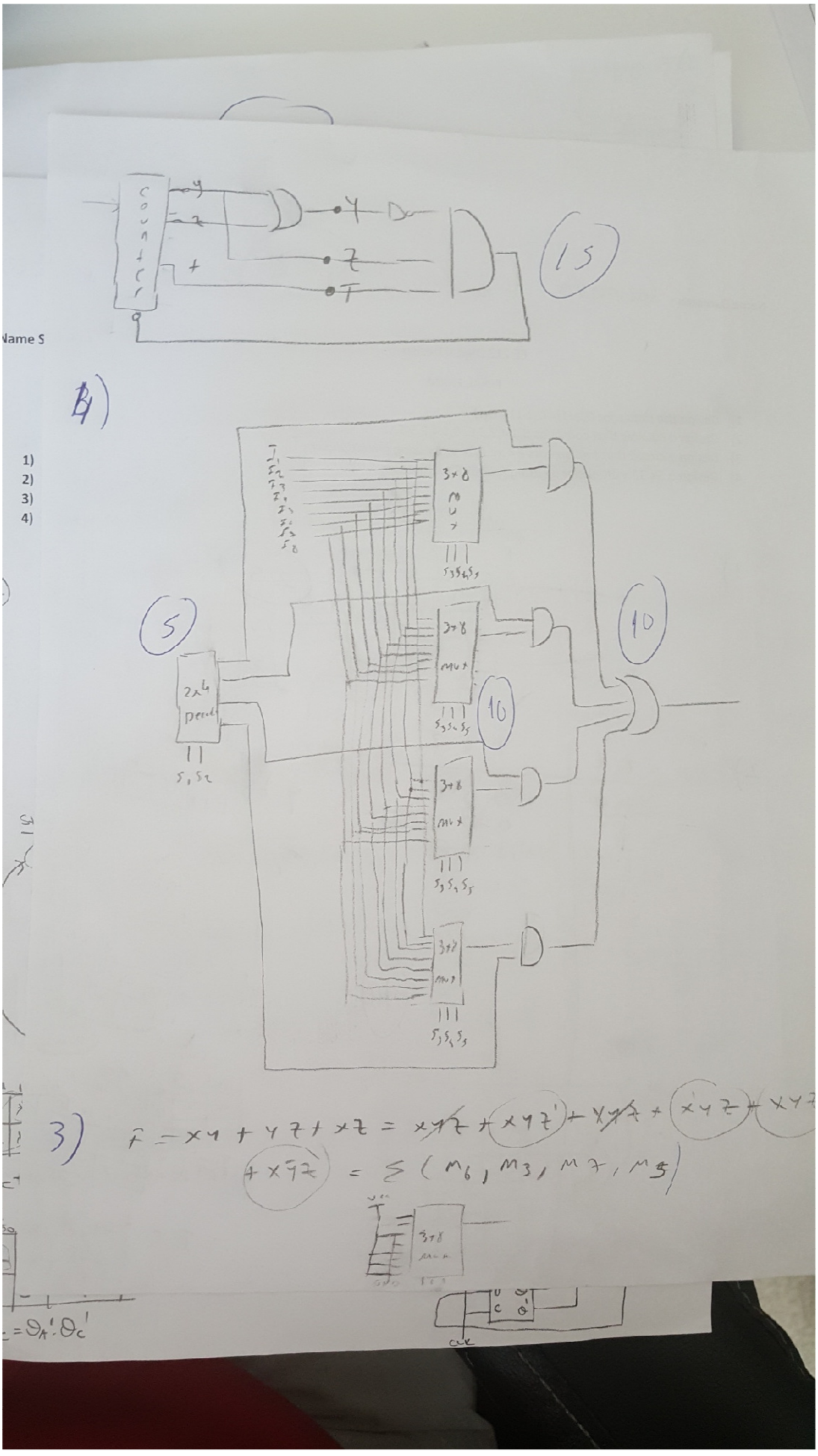
Y = y + z



Z = y



T = t


Name S
B)
1)
2)
3)
4)
COUNTER
15
5
10
10
2x4 DEMUX
3x8 MUX
3) F = xy + yz + xz = xyz + xyz' + xyz + x'yz + xyz
+ xz = Σ(m6, m3, m7, m5)

Name Surname :

11.12.2021

Student ID :

2020-2021

FALL

EE 213 FINAL EXAM

Q1) a) 34p Please design and DRAW the circuit of output for the REDUCED state table (if it is reducable) form of the given state table given below.

Present State	Next State (input=0)	Next State (input=1)	Output (input=0)	Output (input=1)
00	11	10	01	01
01	01	10	11	11
10	10	01	00	10
11	01	10	11	11

Q2) 33 p Please design a circuit that has a red led and a blue led and simulates a police light (i.e : The red led turns on and off periodically and it gives light when the blue one doesn't, then it turns off when the blue one turns on.)

Q3) 33 p Design a counter that counts upto 3 and back down to 0 such as ; 0,1,2,3,2,1,0,1,2,3,2,1,0…

Name Surname : SOLUTIONS

Student ID :

11.12.2021

2020-2021

FALL

EE 213 FINAL EXAM

Q1) a) 34p Please design and DRAW the circuit of output for the REDUCED state table (if it is reducable) form of the given state table given below.

	Present State	Next State (input=0)	Next State (input=1)	Output (input=0)	Output (input=1)
0	00	~~11~~ 01	10	~~01~~ 00	~~01~~ 00
1	~~01~~	~~01~~	~~10~~	~~11~~ 01	~~11~~ 01
2	10	10	01 00	00	10
3	~~11~~	~~01~~	~~10~~	~~11~~	~~11~~

Q2) 33 p Please design a circuit that has a red led and a blue led and simulates a police light (i.e : The red led turns on and off periodically and it gives light when the blue one doesn't, then it turns off when the blue one turns on.)

Q3) 33 p Design a counter that counts upto 3 and back down to 0 such as ; 0,1,2,3,2,1,0,1,2,3,2,1,0...

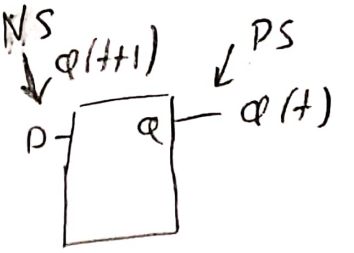
SOLUTIONS

1) line 1 and 3 are same, line 3 will be cancelled and all 11's will be 01 on remaining ports Then, line 0 and 1 become same and line 1 will be cancelled, and all 01's will be 00 on remaining ports, new state table becomes

PS	NS I=0	NS I=1	Out I=0	Out I=1
00	01	10	00	00
10	10	00	00	10

Extending it;

PS-I q_1 q_0		NS D_1 D_0		Out A_1 A_0	
0	0	0	1	0	0
0	1	1	0	0	0
0	1	0	x	x	x
0	1	1	x	x	x
1	0	0	0	0	0
1	0	1	0	1	0
1	1	0	x	x	x
1	1	1	x	x	x



$D_0 = Q_0(t+1)$

$D_1 = Q_1(t+1)$

for output bits

A_0 =>

q_1 \ $q_0 I$	00	01	11	10
0	0	0	x	x
1	0	0	x	x

$A_0 = 0$

A_1 =>

q_1 \ $q_0 I$	00	01	11	10
0	0	0	x	x
1	0	1	x	x

$A_1 = q_1 \cdot I$

D_1 =>

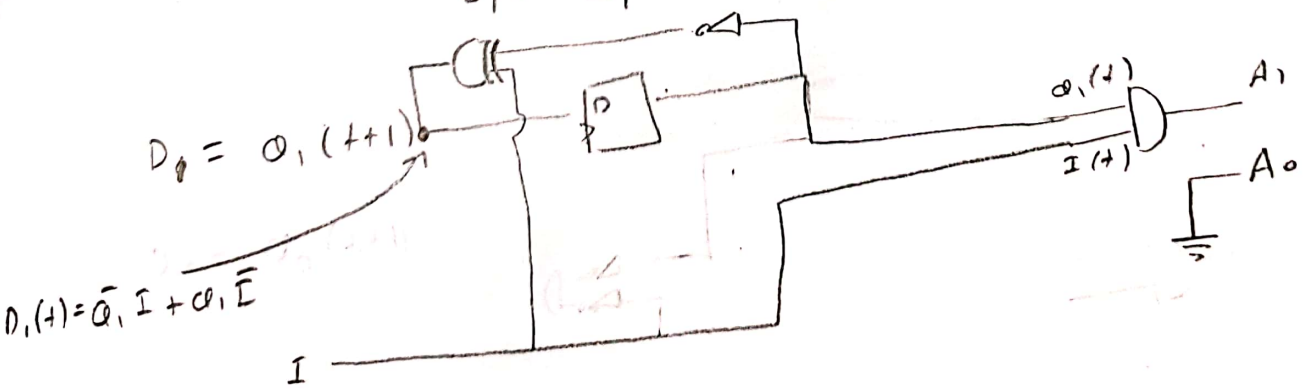
q_1 \ $q_0 I$	00	01	11	10
0	0	1	x	x
1	1	0	x	x

D_0 =>

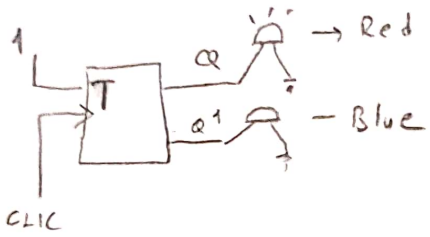
q_1 \ $q_0 I$	00	01	11	10
0	1	0	x	x
1	0	0	x	x

$D_1 = \bar{q}_1 I + q_1 \bar{I}$

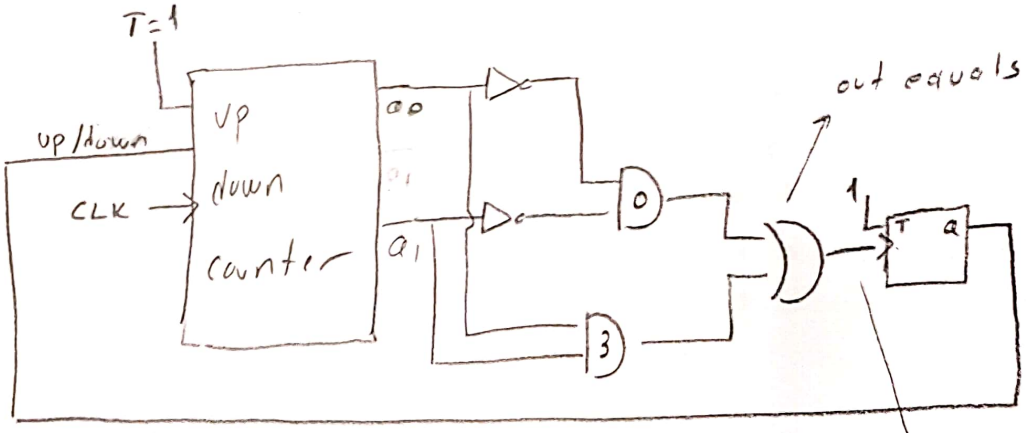
$D_0 = \bar{q}_1 \bar{I}$



2)


1
T
Q
Q'
→ Red
– Blue
CLIC

3)


T=1
up/down
CLK
up
down
counter
q0
q1
0
3
1
T
Q
out equals 0 or 3
clock changes the counting direction

Name Surname : SOLUTIONS
ID

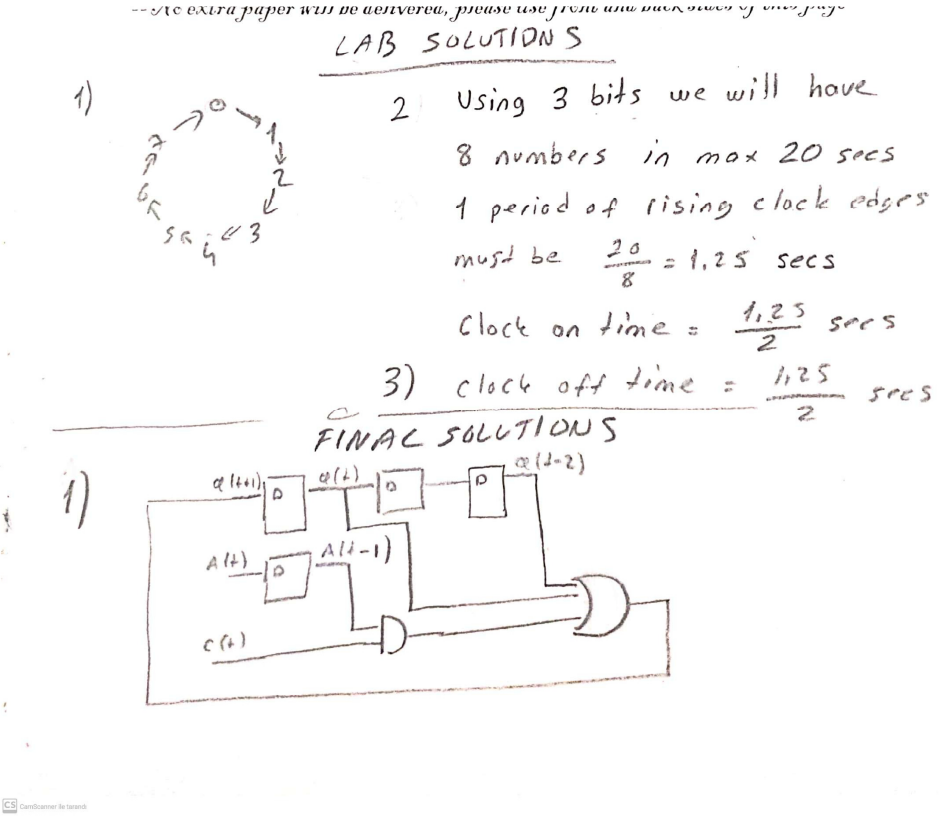
EE 213 LAB Exam 10.01.2022

1) Please draw the state diagram of a 3 bits counter such that it will give the outputs of one period in 20 seconds, and shows exactly one period on the screen.
2) To see the outputs exactly as above what value should the clock on time be adjusted to ?
3) To see the outputs exactly as above what value should the clock off time be adjusted to ?

EE 213 FINAL EXAM

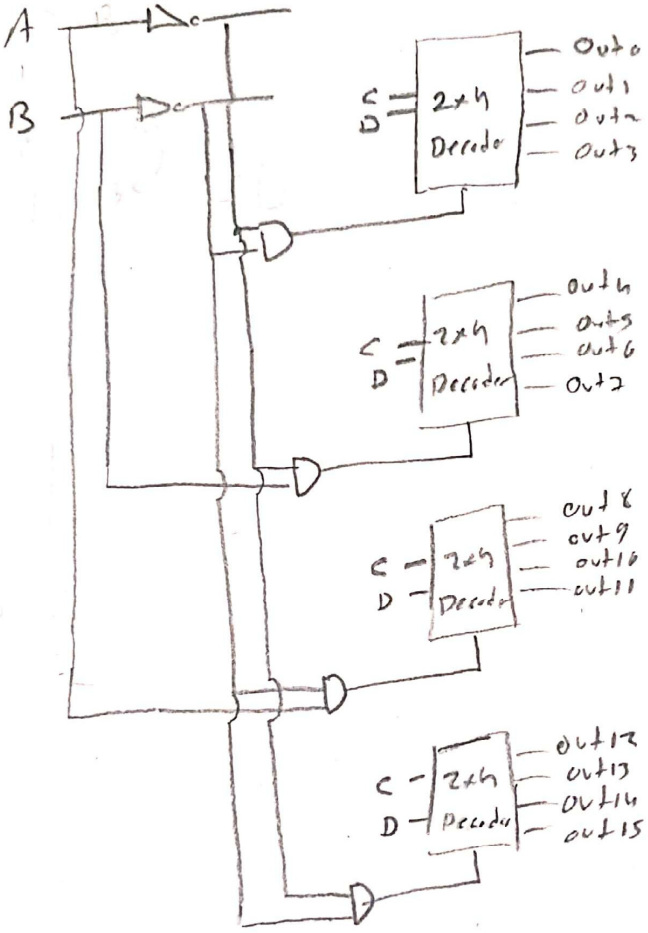
1) Draw the circuit for Q(t+1)=Q(t)+A(t-1).C(t)+Q(t-2)
2) Draw the state diagram of a 3 bits up/down counter.
3) Design a 4x16 decoder using four 2x4 Decoder

--No extra paper will be delivered, please use front and back sides of this page--



2)

3)


A
B
C
D
2x4
Decoder
out0
out1
out2
out3
out4
out5
out6
out7
out8
out9
out10
out11
out12
out13
out14
out15